REMARKS

I. Formal Matters.

Claims 3 and 7-10 are all the claims pending in the application.

Interview Summary. On January 17, 2006, the undersigned initiated a teleconference with Examiner Torres regarding the apparent contradiction in rejections of claim 5. The Examiner rejects claim 5 as being unpatentable over *Mesko* under 35 U.S.C. §103(a) and then acknowledges the deficiency of *Meszko* in the rejection of claim 5 as being unpatenable over *Meszko* in view of *Saito* under 35 U.S.C. §103(a) (FOA dated December 13, 2005, page 9). Corrections to the latter rejection with respect to citations to and application of *Ikegami* are provided in the Supplemental Final Office Action dated January 23, 2006. In the Interview Summary appended to the Supplemental Final Office Action (dated January 23, 2006) of the Examiner notes his decision to maintain two rejections of claim 5. The Supplemental Final Office Action restarts the due date of response for the Final Office Action mailed December 13, 2005 to January 23, 2006 (Interview Summary page 3).

II. Claims.

The Examiner maintains the rejection of claims 3 and 10 as allegedly being unpatentable over *Meszko* in view of *Igarashi, et al.* (U.S. Patent No. 6,466,632 B1) under 35 U.S.C. §103(a).

In response to previously submitted arguments, the Examiner asserts that Applicant contends that "*Mesko* fails to provide controlling delay circuits on the basis of the comparison signal." (OA page 2). However, Applicant actually asserted and the Examiner acknowledged that "*Meszko* fails to disclose that the delay amount control circuit calculates an average

amplitude of the comparison signal output from said comparator, and controls said delay circuits so that the average amplitude is equal to or lower than a threshold value, whereby the difference in delay times between said two transmission units is converged to a permissible and acceptable value range" (OA dated August 18, 2005 at page 3; Amendment filed November 17, 2005 at page 6).

The Examiner continues to acknowledge that "*Meszko* fails to disclose that the delay amount control circuit calculates an average amplitude of the comparison signal output from said comparator, and controls said delay circuits so that the average amplitude is equal to or lower than a threshold value, whereby the difference in delay times between said two transmission units is converged to a permissible and acceptable value range" (OA pages7-8). The Examiner asserts that "the use of an average circuit, usually a low pass filter, and a threshold comparator are very well known." (OA page 8) However, the Examiner does not assert that an averaging circuit and comparator, as utilized in the subject claim, are well known. Therein, the Examiner relies on *Igarashi* to teach the claim subject matter acknowledged to be lacking in *Meszko*. The Examiner asserts that *Igarashi* teaches a delay amount control circuit, calculates an average amplitude of a comparison signal and controls the delay circuits so that the average is below a given threshold (OA page 3). More specifically, the Examiner cites to *Igarashi* at Fig. 16 and col. 15, line 40 to col. 16, line 29 (OA page 8).

Turning to *Igarashi* at col. 15 lines 40-45, we find that *Igarashi* discloses an averaging circuit 74 and a comparison circuit 75 in Fig. 16. Further, *Igarashi* teaches that adder 73 adds *received* signal powers 701 and 702 to obtain a sum of received signal powers 703. Averaging

circuit 74 averages the sums (703) for a period of time to obtain an average sum *received* signal power, which is then compared to a threshold value (*Igarashi* col. 15, lines 56-62).

In contrast, claim 3 requires, comparing detected [transmission] signals and generating a comparative signal. And then, calculating an average amplitude of comparison signals output from the comparator. *Meszko* fails to teach comparing detected signals, generating a comparative signal, and calculating an average amplitude of comparison signals (OA page 3). Secondary reference *Igarashi* fails to provide this deficiency (*Igarashi* col. 15, lines 56-62).

Igarashi teaches summing received signal powers and averaging sums, and then comparing the averaged signal to a threshold, therein *determining the selection of either a diversity reception circuit, or the output of a least squares combining circuit* (col. 15 line 50 -col. 16, line 7). In contrast, claim 3 requires, "*controlling the delay circuits* on the basis of the comparison signal so that modulation timing of RF signals to be transmitted from said two transmission units are coincident to each other". *Meszko* fails to provide controlling delay circuits on the basis of the comparison signal *wherein the delay amount control circuit calculates an average amplitude of the comparison signal output from said comparator*, and controls said delay circuits (OA page 3). Secondary reference, *Igarashi* fails to provide this deficiency; where *Igarashi* teaches averaging summed received signals *to select* a best signal quality from the available outputs. *Meszko* and *Igarashi*, either alone or in combination, fail to teach or suggest each and every element required by claim 3. At least for this deficiency, the rejection of claim 3 as being unpatentable over *Meszko* in view of *Igarashi* under 35 U.S.C. §103(a) should be withdrawn.

Claim 10 is asserted as being allowable at least by virtue of its dependence upon an allowable claim.

Claim 5 is rejected as allegedly being unpatenable over *Meszko* in view of *Saito, et al.* (U.S. Patent No. 5,943362) under 35 U.S.C. §103(a). Claim 5 is rejected as being unpatentable over *Meszko* under 35 U.S.C. §103(a). Claim 5 is canceled via this amendment without prejudice or disclaimer for the purpose of expediting allowance of the subject application.

Claims 5, 7 and 8 are rejected as being unpatentable over *Meszko* under 35 U.S.C. §103(a).

As noted above, claim 5 is canceled via this amendment without prejudice or disclaimer for the purpose of expediting allowance of the subject application.

Claim 7. The Examiner asserts that the single block enclosing a filter, an upconverter, and an amplifier *behind* the delay block demonstrates that the position of the delay block relative to a frequency converter or relative to an amplifier is patentably insignificant (*Meszko*, Fig. 1). Therefore, the Examiner asserts the required claim subject matter of " . . . said delay circuit is provided *between* said frequency converter and said amplifier . . ." is obvious in view of *Meszko* (claim 7; FOA pages 11-12; OA dated August 18, 2005 page 6).

Clearly *Meszko* fails to teach or disclose a delay unit between a frequency converter and an amplifier. Is a delay circuit between a frequency converter and an amplifier obvious? No.

"The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims [being rejected] is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without

the benefit of appellant's specification, to make the necessary changes in the reference device." (*Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984; MPEP §2144.04(VI)(C)). And therein the Examiner fails to make a prima facie case of obviousness. In *Meszko*'s Fig. 1 the delay circuit is clearly shown and described as preceding all three , the filter, upconverter and amplifier (col. 3 line 41- col. 4 line 4). *Meszko* fails to suggest either in Figures or in the text that a delay circuit is provided between said frequency converter and said amplifier.

The Examiner asserts that placing the delay circuit between the upconverter and the filter "*will not change the signal"* as compared to placing the delay circuit before the filter, upconverter and amplifier. Further, the Examiner asserts that this is a "fact" (FOA page OA dated August 18, 2005, page 7). In the present office action the Examiner asserts that placing the delay circuit between the upconverter and the filter will not "change the operation of the device" is a "fact" (FOA page 12). The Examiner turns to Figs. 1 and 3 for evidentiary support of his asserted "fact(s)". The Examiner asserts that Figs. 1 and 3, which depict the filter, upconverter and filter as a single block diagram, implies that it would not make any difference to place the delay circuit between the upconverter and the filter.

Applicant asserts that the block diagrams of Figs. 1 and 3 do not even imply that the positions of the three components therein (filter, upconverter, and amplifier) relative to each other are interchangeable. It is well known by one of ordinary skill in the art that filtering after amplifying will diminish aliasing[1], and therefore the sequence of filtering and amplifying matter

[1] http://www.maxim-ic.com/appnotes.cfm/appnote_number/928.

significantly. The same Figs. fail to imply or provide evidentiary support that an element external to the subject block interjected into the block, would not modify the operation, or signal processing, of at least the subject block.

Meszko fails to suggest either in Figures or in the text that a delay circuit is provided between said frequency converter and said amplifier and the Examiner fails to make a prima facie case of obviousness for failing to provide a motivation to modify the disclosure in *Meszko* to arrive at required claim subject matter. At least for this deficiency, the rejection of claim 7 as being obvious over *Meszko* under 35 U.S.C. §103(a) should be withdrawn.

Claim 8. The Examiner makes an analogous assertion of obviousness in rejecting claim 8 as discussed above in the traversal of the rejection of claim 7 (FOA page 12). The Examiner asserts that the required claim subject matter of " . . . said delay circuit is provided at the output side of said amplifier . . ." is obvious in view of *Meszko* (claim 8; OA page 12; *Meszko* Fig. 1). As demonstrated above, *Meszko* shows in Fig. 1 and describes in the associated text that the delay circuit precedes the combination of a filter, an upconverter, and an amplifier. While the arrangement of the elements of the combination is not specified, the placement of the delay circuit as preceding the combination is clearly disclosed and taught (*Meszko* Fig. 1 col. 3 lines 40- col. 4, line 4). *Meszko* fails to teach or suggest a delay circuit on the output side of the amplifier. In fact, *Meszko* arguably teaches away from the subject matter of claim 8 by teaching and disclosing a delay circuit on the input side of the amplifier.

The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." (*Ex*

parte Chicago Rawhide Mfg. Co., 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984; MPEP §2144.04(VI)(C)). Therein the Examiner fails to make a prima facie case of obviousness. *Meszko* fails to suggest either in Figures or in the text that a delay circuit is provided on the output side of said amplifier. At least for this deficiency, the rejection of claim 8 as being obvious over *Meszko* under 35 U.S.C. §103(a) should be withdrawn

II. Allowable Subject Matter.

Applicant thanks the Examiner for indicating that claim 9 is allowable.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

/Howard L. Bernstein Reg. No. 25,665/
Howard L. Bernstein
Registration No. 25,665

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: April 6, 2006